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Design of Controller IC for Asynchronous Conditioning Circuit of an Electrostatic Vibration Energy Harvester

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Abstract—This paper presents a transistor-level design of a power management electrical circuit for asynchronous electrostatic energy harvester. The conditioning circuit of the harvester is based on a charge pump and a flyback circuits. The designed power management block implements the concept of adaptive behaviour of energy harvester, allowing it to operate in an optimal mode in environment where the magnitude of the vibrations may change in time. For the first time, such a system is designed to operate at high voltage (up to 30 V). However, this paper does not concern the design of electromechanical transducer. The IC design has been carried out in 0.35um highvoltage CMOS technology, and has been validated by a coupled VHDL-AMS/SPICE simulation. The control system average power consumption is less then 0.9uW, whereas the average harvested power is approximately 1.1uW for 14V operation voltage.

Keywords-electrostatic vibration energy harvesting; power management; IC design; low power; high voltage; calibration; MEMS.

The use of electrostatic vibration energy harvester (VEH) based on MEMS variable capacitor, which acts as the kinetic-to-electric energy transducer, requires a conditioning circuit (CC) for power processing [3], [4]. The design of CC is submitted to many restrictions, mainly, concerning the low power consumption. There exist CCs operating either in continuous (asynchronous) or switched (synchronous) mode. Synchronous CCs have been exploited in numerous studies and there exist a few successful implementations of such circuits [7], [9]. The main advantage of asynchronous CC is that it is independent of the frequency of mechanical vibrations, and, hence, its operation does not require a costly precise sensing and control electronics. This study is applied for the asynchronous type of CC, which architecture was priory proposed by B.Yen [8]. The circuit consists of a charge pump and an inductor-based flyback circuit, which is similar to a buck DC-DC converter. The flyback is connected to a charge pump by a switch SW as shown in Fig. 1. The charge pump achieves the electromechanical energy conversion. The circuit consists of three capacitors and two diodes. C_{res} is a large reservoir capacitor, which provides an initial energy to the system, C_{var} is the variable capacitor (the smallest of three capacitors), which operates

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Figure 1. Asynchronous CC based on charge pump and flyback topologies.

between C_{max} and C_{min} following the external vibrations phase, C_{store} is a small storage capacitor, which is used for temporary storage of an electrical charge during the electromechanical conversion process. As external vibrations cause a mechanical motion of variable capacitor's plates, C_{var} varies, resulting in variation of the voltage across capacitor under conditions of a constant charge. The diodes D1and D2 act as unidirectional "passive" electrical switches, which synchronize the charge flow from C_{res} on C_{var} and from C_{var} on C_{store} . Hence, a variable capacitor operates as a charge pump, transferring electrical charges and the energy from C_{res} on C_{store} . Since $C_{res} >> C_{store}$, during pumping V_{res} barely decreases and only the increase of V_{store} represents the accumulation of the converted energy. Thin curves in fig. 2a),b) show a typical evolution of V_{store} and harvested average power over the vibration period. After several cycles charge pump saturates, i.e. D_2 is no more capable to be forward biased causing the loosing of the further mechanical energy harvested by C_{var} . To continue the process of effective charge pumping, the difference between V_{store} and V_{res} must be reduced. This is done by a flyback circuit operating similarly to a single-input singleoutput (SISO) buck DC-DC converter. As soon as a flyback circuit is being activated by a switch SW, electrical charges, as well as the accumulated energy, on C_{store} is transferred to C_{res} via the inductor L and the free-wheeling diode D_{fly} . The flyback operation is a wasteful process due to



Figure 2. VEH operation curves: a) Vstore; b) Harvesting power cycle.

constitutive energy losses in SW, L and control electronics. Hence, it should occur only when C_{store} has accumulated sufficient energy. The fundamental challenge consists in the determination of the optimal flyback switching sequence, that affects the overall system performance. Recent solution proposed by [5] addresses the definition of the optimal values of C_{store} and the charge pump cycle number *n*. Another approach that we have shown in [1] consists in operation of the VEH under some optimal range of V_{store} . Thick curves in fig. 2a),b) show the evolution curve of V_{store} between V_1 and V_2 voltage levels, and the corresponding average power produced by a system respectively. V_1 and V_2 are calculated using semi-empirical equations [1]:

$$V_1 = V_{res} + 0.1(V_{store\ max} - V_{res}), V_2 = V_{res} + 0.6(V_{store\ max} - V_{res}).$$
(1)

Here $V_{store\ max}$ is the theoretical maximum of V_{store} , which is close to V_{store} saturation voltage. The behavioral model in [2] highlighted that the systematic update of V_1 and V_2 during a so-called *calibration* phase allows VEH adaptation to unpredictable change of amplitude/frequency of the ambient vibrations. During calibration, the charge pump is forced to run up to the saturation, and hence, $V_{store\ max}$ can be measured and V_1 and V_2 calculated. The calibration related to the energy losses repeats once for many *harvesting* (charge pump+flyback) cycles.

Current paper presents a first circuit-level design of the adaptive concept for the asynchronous CC, which is shown in Fig.1. The main difficulty of controller design is the high voltage operation of the CC (tens of volts). The circuit is designed in high-voltage 0.35 μ m CMOS technology of AustriaMicrosystems.



Figure 3. Proposed energy harvester system

I. PROPOSED VEH SYSTEM

Fig. 3 shows the proposed IC assisting the CC. The designed circuit includes a switch controller and the switch itself with the auxiliary voltage level shifter. However, the interface between the VEH and the load circuit is not addressed in this paper.

A. High-voltage switch

The design of a switch between the charge pump and the flyback circuits presents a severe challenge, since it is a floating switch and it must operate with high voltage with respect to the ground. Its implementation is also restricted by low power consumption. As our theoretical study [2] revealed, in order to drive a flyback switch a complex control electronics is required, operating at standard voltage. It is possible to design a floating switch using a high-voltage PMOS device able to withstand high voltages (up to 50V for AMS 0.35 μ m HV) between its source and drain terminals. However its control voltage Vgs is limited by a low voltage set by the technology process (3.3V). The main issue is that Vgs is referenced to the floating high-voltage source terminal of HV-PMOS and, hence, its control is not straightforward and requires a voltage level shift [5].

The voltage level shifter is the most critical block of the system, mainly, because of the strict power limitations. This requirement is fulfilled with a "zero static consumption" architecture using an *analog memory* to store the state of the VDD-referenced transistor. Inspired from [6] the analog

memory function is ensured with a dynamic RS flip-flop. The state of the flip-flop corresponds to the switch state and it is driven by low-voltage strobe signals *on* and *off*. The power dissipation is mostly limited to the triggering of the flip-flop to its new state.

The sizing of switch itself is a trade-off between the input capacitance as well as conductive and leakage losses. Indeed, PMOS device must have a large channel width and a small length in order to minimize the "on" resistance Rdson. At the same time it should not be too large with intent to keep the input capacitance reasonably low regarding the high-speed performance as well as the power consumption. Theoretical study and simulation results provide us with an optimum transistor size: W=1000 μ m, L=1 μ m. Losses associated with the leakage current through a large channel transistor are about 500pA, that is approximately 15nW (for V_{store} =30V) of power dissipated in static mode.

B. Switch control block

The purpose of the flyback switch control block is the generation of strobe control signals *on* and *off* with a consideration of the "auto-adaptation" algorithm (periodic calibration phase). A power consumption of the controller must obviously be lower then power converted from the mechanical domain, and, hence, power requirement is the main criteria for the design.

A control signal *mode* coordinates the operating conditions of the VEH: either *calibration* mode or *harvesting*. Since the CC is a high-voltage circuit and the controller is a standard voltage logic, high-to-low voltage interface (voltage dividers, level shifter) is included.

Calibration mode: During the calibration, a single block of the controller system is enable - the generator of V_1 and V_2 . It is an analogue calculator sensing V_{res} and V_{store} and performing the calculation of V_1 and V_2 following the formula (1). For further processing the outputs of the calculator are divided with external high resistors (up to 1G Ω) and are stored in relatively large on-chip capacitors (300pF). The division factor is around 12, since the maximum specified V_{store} is limited to 30V and the maximum divided low-voltage is 2.5V.

Harvesting mode: Harvesting mode is a normal longlasting operating phase. Controller implies the detection of two events necessary to open and close the switch. First event relates to the detection of the crossing of V_2 point by V_{store} . At this phase V_{store} is divided with a factor 12 using another off-chip resistors and is compared with V_2 , which was hold during the calibration. Divider and comparator are synchronized with a low-frequency (100Hz) clock *clk*. After the " V_{store} above V_2 " event detection (Q_{V2} is high), the on pulse is generated by a control logic and the switch activates a flyback circuit. At the same moment the signal Q_{V2} enforces the detection of the crossing of V_1 by V_{store} . The duration of the flyback phase is very short (few to tens μ s) in terms of a vibration period, and, hence, requires a continuous time processing. The assisting voltage divider is composed of the series of 12 CMOS diodes due to division speed and power consumption. The operation of the " V_1 cross detection" block is controlled by a state machine.

C. Power consumption

The consumption of the proposed switch controller can be represented as a sum of power dissipated by low-voltage sub-circuits and by high-voltage counterparts. For the lowvoltage the most of energy is consumed by two comparators presented in the system (several hundreds of nA), while power consumption of few logic gates presented in the system can be neglected. Sub-circuits consuming energy from the high-voltage source are resistive and diode dividers, as well as a voltage level shifter with a flyback switch. Voltage dividers made with high-nominal resistors conduct a relatively low current (few to tens nA) during active phase, and they present maximum of 90pA of leakage current through NMOS transistors that act as switches. Diode-made voltage divider consumes few μA current but for a short duration of time (during a flyback phase), whereas it's leakage current in "off state" is represented by about 130 pA (for 30V). The voltage level shifter conduct 3mA current during two strobe signals (each lasts \approx 50ns), and the leakage current mostly related to a large channel HV switch is 500pA for 30V.

II. SIMULATION RESULTS

The overall harvester system was modeled using highvoltage 0.35 μ m AMS transistor models as well as the behavioral transducer model [1] which uses the parameters of the realistic transducer/resonator device presented in [3]. The external vibration frequency is around 250 Hz, the external acceleration amplitude is 1g. The initial voltage on C_{res} is 10V.

Fig. 4(a) presents the transistor-level simulation results for the VEH operation during 50 seconds. The duration of the *mode* pulse (when calibration phase must be active) is 100ms and it repeats every 2 seconds (only for simulation purposes, in practice it should be tens seconds). Accordingly to the plot the voltage V_{res} increases continuously with time that corresponds to the accumulation of the converted energy. Fig. 4(b) is focused on the operation during calibration mode (in the middle) and the harvesting modes before and after update of V_1 and V_2 . During harvesting modes the divided voltage $(V_{st-div-s})$ evaluates between V_2 and V_1 parameters, which are held constant. The division and comparison are processed every clk clock cycle. Fig. 4(c) is a zoom on the flyback phase. It shows the detection of V_1 by V_{store} and the switch controlling. Initially, the SW gate voltage V_{gpsw} equals V_{store} . The on pulse forces V_{gpsw} voltage to become $V_{store}-3V$, turning on the flyback switch. It is important to notice that despite the floating V_{store} ,



Figure 4. Simulation results

 V_{gpsw} is kept constant during flyback, meaning that the switch is reliably closed. Voltage curves in the top present the V_1 crossing detection phase: $V_{st-div-a}$ outputted from the diode voltage divider repeats the behavior of V_{store} , and as soon as $V_{st-div-a}$ crosses the bottom line (V_1 level), the off strobe is produced, opening SW.

III. CONCLUSION

In this paper we proposed a transistor-level circuit design for the asynchronous electrostatic VEH, implementing the adaptive behavior. IC architecture includes a power management control block and a high-voltage switch. The designed circuit corresponds to the ultra-low power consumption requirements (0.9 μ W at 14V on C_{res}), however, the net average power generated on C_{res} under the same voltage is around 1.1 μ W, which is just slightly higher then the power consumption. This figure can be improved using an optimized capacitive transducer, which is not part of current work, and with the maximization of the voltage level on C_{res} . The design was validated by mixed VHDL-AMS/SPICE simulations using the high-voltage 0.35 μ m CMOS process provided by AMS. The implementation of a hard prototype of this circuit is a subject of ongoing work.

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